APPENDIX

1. (New 21)   An   adder   based   circuit   embodied   in   an
integrated circuit comprising

an   input   module   responsive   to   inputs   A[i]   and   B[i]   to
generate a first input function U[i] = A[i]&B[i] and a second
input function V[i] = A[i]$\lor$B[i] or V[i] = A[i]$\oplus$B[i];

a carry module responsive to the first and second input
functions to generate carry functions; and

an output module responsive to the first and second input
functions and the carry function to provide an output function

$$S=\sum_{i=0}^{n-1}2^{i}S[i]\quad S=\sum_{i=0}^{n}2^{i}S[i]\_=\sum_{i=0}^{n-1}2^{i}A[i]\ +\ \sum_{i=0}^{n-1}2^{i}B[i],$$

wherein   the   carry   module   has   a   minimal   depth   defined   by   a
recursive expansion of at least one function associated with the
carry module based at least in part on a ~~variable~~ parameter k,
where k $\geq$= F_l and n-k $\leq$= F_{l-1} and where l satisfies F_l < n
$\leq$= F_{l+1}, F_{l-1}, ~~{~~F_l and F_{l+1} are members of} ~~is~~ a
Fibonacci series and n is the number of bits of at least one of
the inputs.

5. (New 23)   The process of claim 22, wherein step (b)
comprises steps of:

    b1)   defining recursive functions

            h'_l   =   h_l(U[k+1],U[k+2],V[k+2],...,
            U[k+1],V[k+1]) and

            v'_l = V[k+1]&,...,&V[k+1],

            where l = 1,...,n-k and U[i] and V[i] are inputs
            to the carry module, k=F_l and n-k=F_{l-1}, l
            satisfies F_l<n$\leq$=F_{l+1}, {F_l} is the Fibonacci
            series defined recursively from the equality
            F_{l+1}=F{l}+F_{l+1} and n is the number of bits
            of an input to the carry module, and

    b2)   recursively   expanding   the   recursive   functions   to

minimize l.

13. (New 24)   The process of claim 12, wherein step (c) comprises steps of:

   c1)   defining recursive functions

   $H^i\_k = h^{\{i+1\}}\_{\{k-1\}} \vee v^{\{i+1\}}\_{\{k-1\}} \& h^i\_l$

         and

   $v^i\_l = v^{\{i+1\}}\_{\{k^l\}} \& v^i\_l$

         based on a function of the adder based circuit, where k=F_l and n-k=F_{l-1}, l satisfies F_l<n$\leq$=F_{l+1}, {F_l} is the Fibonacci series defined from the equality F_{l+1}=F{l}+F_{l+1} and n is the number of bits of an input to the adder based circuit, and

   c2)   recursively expanding the recursive functions to minimize l.

15. (New 26)   The storage medium of claim ~~14~~ 25, wherein <u>the circuit structure defined by the processor includes a carry module and the second processor executable instructions</u> comprises:

      processor executable instructions that enable the processor to define recursive functions

      $h'\_l = h\_1(U[k+1], U[k+2], V[k+2], \ldots, U[k+1], V[k+1])$ and

      $v'\_l = V[k+1] \&, \ldots, \& V[k+1]$,

      based on a ~~the~~ carry function <u>of the carry module</u>, where k=F_l and n-k=F_{l-1}, l satisfies F_l<n$\leq$=F_{l+1}, {F_l} is the Fibonacci series defined recursively from the equality F_{l+1}=F{l}+F_{l+1} and n is the number of bits of an input to the carry module, and

      processor executable instructions that enable the processor to recursively expand the recursive functions to minimize l.

20. (New 27)   The storage medium of claim ~~14~~ <u>25</u>, further including third processor executable instructions that enable the processor to minimize fanout depth of the adder base circuit, the third processor executable instructions comprising:

 processor executable instructions that enable the processor to define recursive functions

  $H^i\_k = h^{\{i+1\}}\_{\{k-1\}} \vee v^{\{i+1\}}\_{\{k-1\}} \& h^i\_l$

   and

  $v^i\_l = v^{\{i+1\}}\_{\{k^l\}} \& v^i\_l$

  based on a function of the adder based circuit, where $k = F\_l$ and $n-k = F\_{\{l-1\}}$, l satisfies $F\_l < n \leq F\_{\{l+1\}}$, $\{F\_l\}$ is the Fibonacci series defined from the equality $F\_{\{l+1\}} = F\{l\}+F\_{\{l+1\}}$ and n is the number of bits of an input to the adder based circuit, and

 processor executable instructions that enable the processor to recursively expand the recursive functions to minimize l.